|  |
| --- |
| University of new mexico department of electrical and computer engineering |
| 2-1 Multiplexer |
| ECE 321: Electronics I |
| Fall 2012 |
|  |
| **Tony Mancuso, Jeremy McConaha, Brian Becker** |
| **12/5/2012** |

|  |
| --- |
|  |

[[1]](#footnote-1)

ECE 321 Term Project – 2-1 Multiplexor

Brian Becker, Jeremy McConaha, Tony Mancuso

# INTRODUCTION

The ECE 321 Fall 2012 2-1 multiplexer project is intended to provide students with exposure to and hands-on practice in design, manufacturing-layout, PSPICE implementation, and analysis of a semiconductor circuit. Design of the circuit will be accomplished in LEDIT using MOSIS 2 µm Process (SCMOS) technology, and the LEDIT layout will be extracted to a PSPICE file for implementation and characterization. Analysis performed will include verification of circuit operation, worst case switching delay, worst case switching energy, input capacitances, and output resistance. Design considerations, implementation notes, results, and conclusions will be presented in this report.

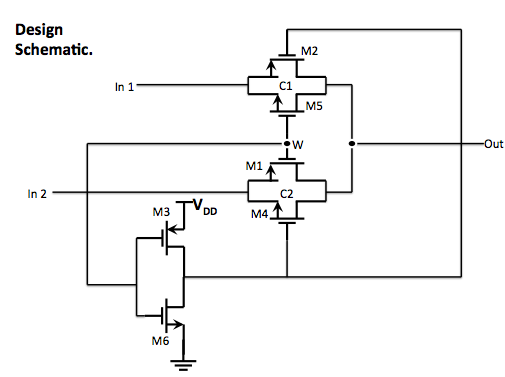
# Design

1. Design Choice:

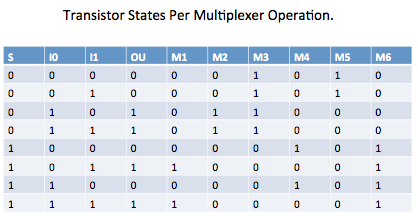
There are many methods by which a 2-1 multiplexer can be assembled. The performance of different options varies in size, power efficiency, speed, and cost. Our team chose to use CMOS transmission gates with the following considerations:

* Simplicity of design.
* Smallest number of components to assure logic integrity.
* Reasonable performance in speed and power consumption.

1. Layout: (total area = 20/76\*10^-9 meters =

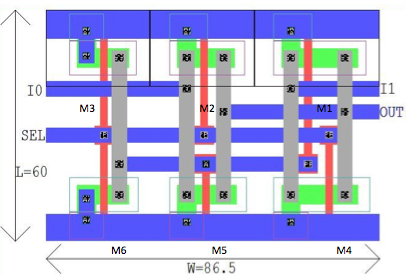
**

*Figure 1:*



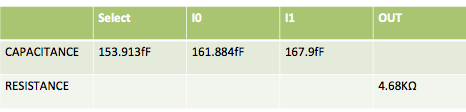
*Figure 2:*

# implementation



*Figure 3: LEDIT Layout with dimensions.*

# Results



*Figure 4:*

# Conclusion

Appendix

1. [↑](#footnote-ref-1)